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PATENT ABSTRACTS OF JAPAN

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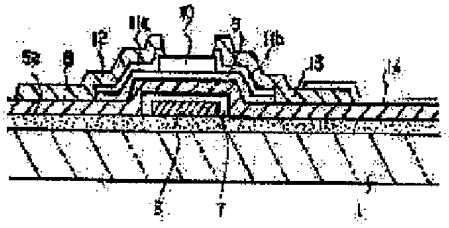
(54) ACTIVE MATRIX WIRING BOARD



(57)Abstract:

PURPOSE: To improve both of hydrofluoric acid resistance and dry etching resistance by using aluminum oxide as an etching protective film.

CONSTITUTION: The etching protective film 5a consisting of the aluminum oxide (Al2O3) is formed on an insulating substrate 1 consisting of glass, etc., and scanning lines 2 having gate electrodes 6 are formed thereon. An oxidized insulating film 7 is formed to cover these electrodes. A gate insulating film 8 is formed to cover this oxidized insulating film 7 and a semiconductor layer 9 thereon. The central part thereof is provided with an etching stopper layer 10. Further, contact layers 11a and 11b are respectively formed on the respective side parts thereof. Source electrodes 12 are patterned and formed on the contact layers 11a and drain electrodes 13 on the contact layer 11b, respectively. The higher hydrofluoric acid resistance and dry etching resistance than the hydrofluoric acid resistance and dry etching resistance of the conventional active matrix wiring substrate formed by using silicon oxide, etc., are obtd. by forming the etching protective film 5a of the aluminum oxide in such a manner.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the structure of the active-matrix wiring substrate used for a liquid crystal display etc.
[0002]
[Description of the Prior Art] The display which comes conventionally to incorporate the active-matrix wiring substrate which prepared a switching element and electrode wiring on substrates, such as a glass plate and a silicon wafer, is put in practical use.
[0003] For example, although the display pattern is formed on a screen by a liquid crystal display's choosing the display picture element arranged in the shape of a matrix, and impressing an electrical potential difference, the active matrix which carries out the selection drive of the display picture element arranged in the shape of a matrix by the switching element as one of the selection methods of such a display picture element, and forms a display pattern is known. He makes the optical modulation of the liquid crystal which intervenes between them occur, and is trying to check this by looking as a display pattern by using a thin film transistor (it calling for short Thin-Film-Transistor and Following TFT.) component, an MIM (metal-insulator layer-metal) component, an MOS transistor component, diode, a varistor, etc. generally, and switching the voltage signal impressed between the picture element electrode of a display picture element, and the counterelectrode which counters this as this switching **.

[0004] Drawing 2 shows an example of a active-matrix wiring substrate typically. On insulating substrates, such as glass, two or more scanning lines 2 and two or more signal lines 3 intersect perpendicularly mutually, and this active-matrix wiring substrate is arranged by parallel, respectively. The picture element electrode 14 which drives liquid crystal, and the switching element 4 which carries out the selection drive of this picture element electrode are formed in each rectangle field surrounded with each scanning line 2 which carries out proximal, and each signal line 3.
[0005] Next, the cross-section configuration of the part containing TFT of the active-matrix substrate using TFT as a switching element 4 is explained based on drawing 3 .
[0006] On the insulating substrates 1, such as glass, etching protective coat 5b which consists of silicon oxide or tantalum oxide is formed on the whole surface. The scanning line which has the gate electrode 6 is formed in besides, this is covered and the oxidation insulator layer 7 is formed. A tantalum, aluminum, etc. are used so that the oxidation insulator layer 7 prepared on it as an ingredient of the scanning line may be formed good with an anode oxidation method. This oxidation insulator layer 7 is covered and the gate dielectric film 8 which consists of SiO2 and Si3N4 grade over the whole substrate surface is formed. On gate dielectric film 8, it is formed so that the semi-conductor layer 9 which consists of a silicon thin film may cover the gate electrode 6. The etching stopper layer 10 is formed in the center section on this semi-conductor layer 9, and contact layer 11a and contact layer 11b are formed in contact with each flank of the semi-conductor layer 9, respectively on each flank of the etching stopper layer 10. On contact layer 11a, pattern formation of the drain electrode 13 with which the source

electrode 12 which consists of Ti consists of Ti on contact layer 11b again is carried out, respectively. In case the etching stopper layer 10 separates the source electrode 12 and the drain electrode 13, it protects the semi-conductor layer 9 from an etching reagent. In part, the picture element electrode 14 of this drain electrode 13 which consists of transparent conductive film, such as ITO, upwards is formed, and the signal line is formed in contact with this on the source electrode 12.

[0007]

[Problem(s) to be Solved by the Invention] Although silicon oxide or tantalum oxide is used as etching protective coat 5b in the above-mentioned TFT matrix substrate silicon oxide -- **** -- -proof -- fluoric acid -- a sex -- low -- TFT -- membrane formation -- the time -- fluoric acid -- depending -- etching -- a stopper -- a layer -- ten -- etching -- a process -- and -- FUTSU -- a nitric acid -- depending -- the source -- an electrode -- (-- Ti --) -- 12 -- etching -- a process -- setting -- as a protective coat -- not functioning -- Moreover, since dry etching-proof nature is low in tantalum oxide In the etching process of the semi-conductor layer 9 and the contact layers 11a and 11b by the plasma-etching process of CF4 and the gate electrode (Ta) 6 by O2 mixed gas and CF4, and O2-/Cl2 mixed gas, it does not function as a protective coat. Therefore, since the active-matrix wiring substrate has received damage in the substrate side when it uses as a liquid crystal display, deterioration of dependability and display grace is invited, or it can become the cause of defect generating.

[0008] This invention is made in order to solve the technical problem of such a conventional technique, and it aims at offering the active-matrix wiring substrate which has the etching protective coat excellent in both fluoric acid-proof nature and dry etching-proof nature by using an aluminum oxide as an etching protective coat.

[0009]

[Means for Solving the Problem] As for the active-matrix wiring substrate of this invention, the above-mentioned purpose is attained because electrode wiring has the protective coat which is arranged two or more in the shape of a matrix on a substrate, and consists of electrode wiring above a substrate from an aluminum oxide in a lower part.

[0010] Moreover, the above-mentioned protective coat is directly formed at least all over one of the two of base substrates, such as a glass substrate and a silicon wafer, and, thereby, as for the active-matrix wiring substrate of this invention, the above-mentioned purpose is attained.

[0011]

[Function] According to this invention, in the etching process at the time of switching element membrane formation, both fluoric acid-proof nature and dry etching-proof nature can be raised by using an aluminum oxide for the etching protective coat of a active-matrix substrate.

[0012]

[Example] Drawing 1 is the sectional view of the part containing TFT of the active-matrix wiring substrate in which one example of this invention which used TFT is shown.

[0013] Etching protective coat 5a which consists of an aluminum oxide (aluminum 2O3) is formed on the insulating substrates 1, such as glass. Besides the scanning line 2 which has the gate electrode 6 is formed, this is covered and the oxidation insulator layer 7 is formed. A tantalum, aluminum, etc. are used so that the oxidation insulator layer 7 prepared on it may be formed with heat or an anode oxidation method good as an ingredient of the scanning line 2. This oxidation insulator layer 7 is covered and the gate dielectric film 8 which consists of Sio2, Si3N4, and Ta2O5 grade over the whole substrate 1 is formed. On gate dielectric film 8, the semi-conductor layer 9 which consists of an amorphous substance or a microcrystal silicon thin film is formed in the location which counters the gate electrode 6 in contact with this. The etching stopper layer 10 which consists of the minerals thin film of Si3N4 grade is formed in the center section on this semi-conductor layer 9, and contact layer 11a and contact layer 11b which consist of an n+-silicon thin film in contact with each flank of the semi-conductor layer 9 are formed on each flank of the etching stopper layer 10, respectively. On contact layer 11a, pattern formation of the drain electrode 13 with which the source electrode 12 which consists of Ti consists of Ti similarly on contact layer 11b again is carried out, respectively. The source electrode 12 and the drain electrode 13 are divided into each by post-etching formed by coincidence. The picture element electrode 14 which

consists of transparent conductive film, such as ITO (In2O3+SnO2) prolonged on gate dielectric film 8, is formed from the edge of this drain electrode 13, and the signal line is formed in contact with this on the source electrode 12.

[0014] Such a active-matrix substrate is manufactured as follows.

[0015] Etching protective coat 5a of an aluminum oxide is directly formed all over one side by the thickness of 500nm by the sputtering method on a glass substrate 1. At this time, the target of sputtering forms the aluminum-oxide film by RF magnetron sputtering using an aluminum-oxide target. Besides, a tantalum is formed by the thickness of 300nm by the sputtering method, and pattern formation of the scanning line which has the gate electrode 6 with photolithography is carried out. Plasma etching which used the mixed gas of CF4 and O2 performs patternizing. Next, the oxidation insulator layer 7 with a thickness of 300nm is formed on the scanning line 2 which has the gate electrode 6 by the anode oxidation method or the oxidizing [thermally] method. The anode oxidation method was used in this example.

[0016] Next, the laminating of the silicon nitride (Si3N4) is carried out by the plasma-CVD method, and gate dielectric film 8 with a thickness of 300nm is formed. It is also the same as when SiO2, Ta 2O5, Y2O3, and TiO3 grade are used in addition to Si3N4. Thus, insulation is raised by making an insulator layer into multilayer structure. It touches on this gate dielectric film 8, the laminating of the amorphous silicon is carried out by the thickness of 30nm by the plasma-CVD method, and the semi-conductor layer 9 is formed. In contact with this semi-conductor layer 9 top, the laminating of the silicon nitride is carried out by the thickness of 200nm, and pattern formation of the etching stopper layer 10 is carried out with photolithography. Patternizing of the etching stopper layer 10 is performed by etching using fluoric acid. Then, patterning of these is carried out to coincidence with photolithography with the semi-conductor layer 9 which carried out the laminating of the contact layers 11a and 11b which consist of an n+ mold amorphous silicon which added Lynn by the thickness of 50nm by the plasma-CVD method, and carried out the laminating previously. The dry etching which used CF4 and O2-/Cl2 mixed gas performs the patternizing at this time. Furthermore, Ti film is formed by the sputtering method on this, and pattern formation of a signal line, the source electrode 12, and the drain electrode 13 is carried out with photolithography. The patternizing at this time is performed by etching using a FUTSU nitric acid. TFT called a reverse stagger mold by the above is produced on etching protective coat 5a.

[0017] In addition, as an ingredient of a signal line, the source electrode 12 of TFT, and the drain electrode 13 of TFT, metals other than Ti, such as aluminum, Cr, and Mo, may be used with the above-mentioned structure. Next, the transparent electrode film (ITO) which used indium oxide as the principal component is formed by 1000nm in thickness on this Ti film, and pattern formation of the addition capacity (not shown) which branched the picture element electrode 14 and this with photolithography is carried out.

[0018] Thus, compared with the conventional TFT matrix substrate with which silicon oxide or tantalum oxide was used for the manufactured TFT matrix substrate as etching protective coat 5a, high fluoric acid-proof nature and dry etching-proof nature were obtained.

[0019]

[Effect of the Invention] As mentioned above, as explained in full detail, both low dry etching-proof nature seen by the etching protective coat of the low fluoric acid-proof nature and tantalum oxide which were seen by the etching protective coat of silicon oxide is improvable by using an etching protective coat as an aluminum oxide according to this invention.

[0020] Therefore, in the active-matrix wiring substrate of this invention, the damage to the substrate by the etching process is small, and generating of the malfunction of the switching element at the time of using as a liquid crystal display, an open circuit, etc. can also be reduced.

[Translation done.]

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TECHNICAL FIELD

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PRIOR ART

[Description of the Prior Art] The display which comes conventionally to incorporate the active-matrix wiring substrate which prepared a switching element and electrode wiring on substrates, such as a glass plate and a silicon wafer, is put in practical use.
[0003] For example, although the display pattern is formed on a screen by a liquid crystal display's choosing the display picture element arranged in the shape of a matrix, and impressing an electrical potential difference, the active matrix which carries out the selection drive of the display picture element arranged in the shape of a matrix by the switching element as one of the selection methods of such a display picture element, and forms a display pattern is known. He makes the optical modulation of the liquid crystal which intervenes between them occur, and is trying to check this by looking as a display pattern by using a thin film transistor (it calling for short Thin-Film-Transistor and Following TFT.) component, an MIM (metal-insulator layer-metal) component, an MOS transistor component, diode, a varistor, etc. generally, and switching the voltage signal impressed between the picture element electrode of a display picture element, and the counterelectrode which counters this as this switching **.

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EFFECT OF THE INVENTION

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TECHNICAL PROBLEM

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MEANS

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OPERATION

[Function] According to this invention, in the etching process at the time of switching element membrane formation, both fluoric acid-proof nature and dry etching-proof nature can be raised by using an aluminum oxide for the etching protective coat of a active-matrix substrate.

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EXAMPLE

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fluoric acid. Then, patterning of these is carried out to coincidence with photolithography with the semi-conductor layer 9 which carried out the laminating of the contact layers 11a and 11b which consist of an n+ mold amorphous silicon which added Lynn by the thickness of 50nm by the plasma-CVD method, and carried out the laminating previously. The dry etching which used CF4 and O2-/Cl2 mixed gas performs the patternizing at this time. Furthermore, Ti film is formed by the sputtering method on this, and pattern formation of a signal line, the source electrode 12, and the drain electrode 13 is carried out with photolithography. The patternizing at this time is performed by etching using a FUTSU nitric acid. TFT called a reverse stagger mold by the above is produced on etching protective coat 5a.

[0017] In addition, as an ingredient of a signal line, the source electrode 12 of TFT, and the drain electrode 13 of TFT, metals other than Ti, such as aluminum, Cr, and Mo, may be used with the above-mentioned structure. Next, the transparent electrode film (ITO) which used indium oxide as the principal component is formed by 1000nm in thickness on this Ti film, and pattern formation of the addition capacity (not shown) which branched the picture element electrode 14 and this with photolithography is carried out.

[0018] Thus, compared with the conventional TFT matrix substrate with which silicon oxide or tantalum oxide was used for the manufactured TFT matrix substrate as etching protective coat 5a, high fluoric acid-proof nature and dry etching-proof nature were obtained.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The sectional view in the part containing TFT of the TFT matrix substrate in which one example of this invention is shown.
[Drawing 2] The top view of the conventional common active-matrix substrate.
[Drawing 3] The sectional view in the part containing TFT of the conventional TFT matrix substrate.
[Description of Notations]
1 Glass Substrate
2 Scanning Line
3 Signal Line
4 Switching Element
5a Etching protective coat (aluminum oxide)
5b Etching protective coat
6 Gate Electrode
7 Oxidation Insulator Layer
8 Gate Dielectric Film
9 Semi-conductor Layer
10 Etching Stopper Layer
11a, 11b Contact layer
12 Source Electrode
13 Drain Electrode
14 Picture Element Electrode

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CLAIMS

[Claim(s)]
[Claim 1] The active-matrix wiring substrate characterized by making the etching-proof nature protective coat to which-two or more electrode wiring is arranged in the shape of a matrix on a substrate, and changes from an aluminum oxide in a lower part from said electrode wiring more nearly up than said substrate intervene.
[Claim 2] The active-matrix wiring substrate according to claim 1 with which the etching-proof nature protective coat is directly formed all over one side of a substrate.

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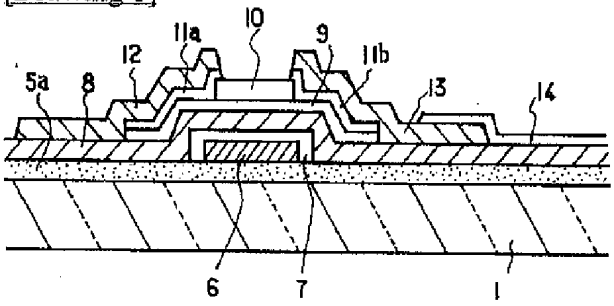
DRAWINGS

[Drawing 1]



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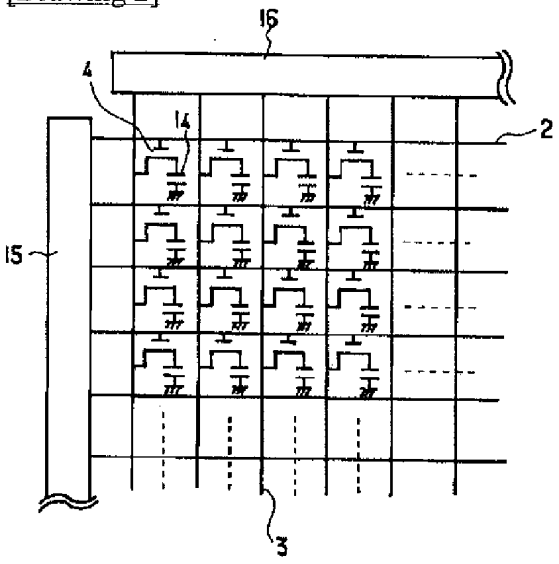
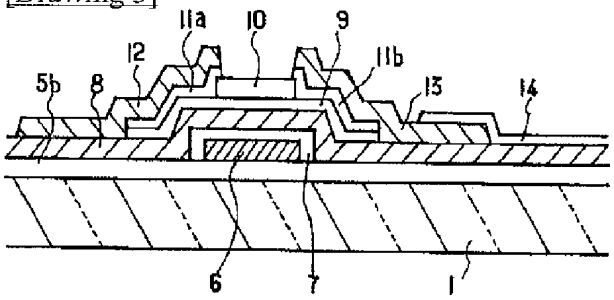


[Drawing 3]



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Ref.4

対応なし、英抄

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号

特開平6－281956

(43)公開日　平成6年(1994)10月7日

(51)Int.Cl.[5]	識別記号	庁内整理番号	ＦＩ	技術表示箇所
Ｇ０２Ｆ　1/136	５００	9119－2Ｋ		
Ｈ０１Ｌ　29/784				
		9056－4Ｍ	Ｈ０１Ｌ　29/78　３１１　Ｘ	

審査請求　未請求　請求項の数２　ＯＬ　（全　４　頁）

(21)出願番号　特願平5－70075

(22)出願日　平成５年(1993)３月29日

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(72)発明者　平田　貢祥
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(74)代理人　弁理士　梅田　勝

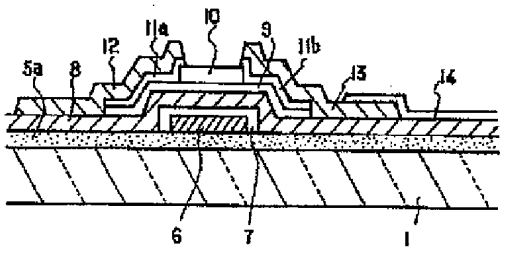
最終頁に続く

(54)【発明の名称】　アクティブマトリクス配線基板

(57)【要約】

【構成】　基板上にマトリクス上に配設された電極配線の下方で基板より上方に酸化アルミニウムから成る耐エッチング性保護膜を介在させ、この上にゲート電極、ゲート絶縁膜、半導体層、エッチングストッパー層、コンタクト層、ソース電極及びドレイン電極から成る逆スタガー型のＴＦＴをフッ酸エッチング液を用いた湿式エッチング及びドライエッチングで形成する。

【効果】　酸化アルミニウムを耐エッチング性保護膜として用いることにより湿式及びドライエッチングに起因する不良を抑制する。



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【特許請求の範囲】

【請求項１】　電極配線が基板上にマトリクス状に複数本配設され、前記電極配線より下方で前記基板より上方に酸化アルミニウムから成る耐エッチング性保護膜を介在させたことを特徴とするアクティブマトリクス配線基板。

【請求項２】　耐エッチング性保護膜が基板の片側全面に直接形成されている請求項１記載のアクティブマトリクス配線基板。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、液晶表示装置などに用いられるアクティブマトリクス配線基板の構造に関する。

【０００２】

【従来の技術】従来より、ガラス板やシリコンウェハなどの基板上にスイッチング素子及び電極配線を設けたアクティブマトリクス配線基板を組み込んでなる表示装置が実用化されている。

【０００３】例えば、液晶表示装置は、マトリクス状に配列された表示絵素を選択して電圧を印加することにより画面上に表示パターンを形成しているが、このような表示絵素の選択方式の一つとして、マトリクス状に配列された表示絵素をスイッチング素子により選択駆動して表示パターンを形成するアクティブマトリクス方式が知られている。このスイッチング素としては、薄膜トランジスタ（Ｔｈｉｎ－Ｆｉｌｍ－Ｔｒａｎｓｉｓｔｏｒ、以下ＴＦＴと略称する。）素子、ＭＩＭ（金属－絶縁膜－金属）素子、ＭＯＳトランジスタ素子、ダイオード、バリスター等が一般に用いられており、表示絵素の絵素電極とこれに対向する対向電極との間に印加される電圧信号をスイッチングすることにより、その間に介在する液晶の光学的変調を生起させ、これを表示パターンとして視認するようにしている。

【０００４】図２はアクティブマトリクス配線基板の一例を模式的に示したものである。このアクティブマトリクス配線基板は、ガラスなどの絶縁性基板の上に複数の走査線２と複数の信号線３とが互いに直交してそれぞれ平行に配設されている。隣設する各走査線２と各信号線３とで囲まれるそれぞれの矩形領域には液晶を駆動する絵素電極１４と、この絵素電極を選択駆動するスイッチング素子４とが設けられている。

【０００５】次に、スイッチング素子４としてＴＦＴを用いたアクティブマトリクス基板のＴＦＴを含む部分の断面構成を図３に基づいて説明する。

【０００６】ガラスなどの絶縁性基板１の上に、酸化ケイ素あるいは酸化タンタルよりなるエッチング保護膜５ｂが全面に形成されている。この上にはゲート電極６を有する走査線が形成されており、これを覆って酸化絶縁膜７が設けられている。走査線の材料としてはその上に

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設けられる酸化絶縁膜７が陽極酸化法で良好に形成されるよう、タンタル、アルミニウムなどが用いられる。この酸化絶縁膜７を覆って、基板全面にわたってＳｉO_2，Ｓｉ，N_4等から成るゲート絶縁膜８が設けられている。ゲート絶縁膜８の上にはシリコン薄膜から成る半導体層９がゲート電極６を覆うように形成されている。この半導体層９の上の中央部にはエッチングストッパー層１０が設けられており、エッチングストッパー層１０の各側部上には半導体層９の各側部に接してコンタクト層１１ａおよびコンタクト層１１ｂがそれぞれ形成されている。コンタクト層１１ａの上にはＴｉから成るソース電極１２が、またコンタクト層１１ｂの上にはＴｉから成るドレイン電極１３がそれぞれパターン形成されている。エッチングストッパー層１０はソース電極１２とドレイン電極１３を分離する際にエッチング液から半導体層９を保護する。このドレイン電極１３の一部上にはＩＴＯ等の透明導電性膜から成る絵素電極１４が形成されており、ソース電極１２の上にはこれに接して信号線が形成されている。

【０００７】

【発明が解決しようとする課題】上記のＴＦＴマトリクス基板では、エッチング保護膜５ｂとして酸化ケイ素あるいは酸化タンタルが用いられているが、酸化ケイ素では耐フッ酸性が低く、ＴＦＴ成膜時のフッ酸によるエッチングストッパー層１０のエッチング工程およびフッ硝酸によるソース電極（Ｔｉ）１２のエッチング工程において保護膜として機能せず、また酸化タンタルでは耐ドライエッチング性が低いので、CF_4，O_2混合ガスによるゲート電極（Ｔａ）６のプラズマエッチング工程およびCF_4，O_2／Cl_2混合ガスによる半導体層９とコンタクト層１１ａ，１１ｂのエッチング工程において保護膜として機能しない。従って、液晶表示装置として用いた場合、アクティブマトリクス配線基板が基板側に損傷を受けているため、信頼性及び表示品位の低下を招来しあるいは不良発生の原因となり得る。

【０００８】本発明は、このような従来技術の課題を解決するためになされたものであり、エッチング保護膜として酸化アルミニウムを用いることにより、耐フッ酸性および耐ドライエッチング性の両方に優れたエッチング保護膜を有するアクティブマトリクス配線基板を提供することを目的とする。

【０００９】

【課題を解決するための手段】本発明のアクティブマトリクス配線基板は、電極配線が基板上にマトリクス状に複数本配設され、電極配線より下方で基板の上方に酸化アルミニウムよりなる保護膜を有することで上記の目的が達成される。

【００１０】また、本発明のアクティブマトリクス配線基板は、上記保護膜がガラス基板、シリコンウェハなどのベース基板の少なくとも片方の全面に直接形成されて

おり、これにより上記目的が達成される。

【0011】

【作用】本発明によれば、アクティブマトリクス基板のエッチング保護膜に酸化アルミニウムを用いることにより、スイッチング素子成膜時のエッチング工程において、耐フッ酸性および耐ドライエッチング性の両方を向上させることができる。

【0012】

【実施例】図1はTFTを用いた本発明の1実施例を示すアクティブマトリクス配線基板のTFTを含む部分の断面図である。

【0013】ガラスなどの絶縁性基板1の上に酸化アルミニウム（Al_2O_3）よりなるエッチング保護膜5aが形成されている。この上にゲート電極6を有する走査線2が形成されており、これを覆って酸化絶縁膜7が設けられている。走査線2の材料としては、その上に設けられる酸化絶縁膜7が良好に熱又は陽極酸化法で形成されるよう、タンタル、アルミニウムなどが用いられる。この酸化絶縁膜7を覆って、基板1の全体にわたってSiO_2，Si_3N_4，Ta_2O_5等から成るゲート絶縁膜8が設けられている。ゲート絶縁膜8の上にはこれに接してゲート電極6に対向する位置に非晶質又は微結晶シリコン薄膜からなる半導体層9が形成されている。この半導体層9の上の中央部にはSi_3N_4等の無機質薄膜から成るエッチングストッパー層10が設けられており、エッチングストッパー層10の各側部上には半導体層9の各側部に接してn⁺－シリコン薄膜から成るコンタクト層11aおよびコンタクト層11bがそれぞれ形成されている。コンタクト層11aの上にはTiから成るソース電極12が、またコンタクト層11bの上には同様にTiから成るドレイン電極13がそれぞれパターン形成されている。ソース電極12とドレイン電極13は同時に成膜された後エッチングで各々に分離される。このドレイン電極13の端部よりゲート絶縁膜8上に延びるITO（$In_2O_3+SnO_2$）等の透明導電性膜からなる絵素電極14が形成されており、ソース電極12の上にはこれに接して信号線が形成されている。

【0014】このようなアクティブマトリクス基板は以下のように製作される。

【0015】ガラス基板1の上にスパッタリング法により、酸化アルミニウムのエッチング保護膜5aを500nmの厚みで片側全面に直接形成する。この時、スパッタリングのターゲットは酸化アルミニウムターゲットを用い、RFマグネトロンスパッタにより酸化アルミニウム膜を成膜する。この上にスパッタリング法によりタンタルを300nmの厚みで成膜し、フォトリソグラフィーによりゲート電極6を有する走査線をパターン形成する。パターン化はCF_4，O_2の混合ガスを用いたプラズマエッチングにより行なう。次に、陽極酸化法または熱酸化法によりゲート電極6を有する走査線2の上に、300nmの厚みの酸化絶縁膜7を形成する。本実施例では陽極酸化法を用いた。

【0016】次に、プラズマCVD法により窒化ケイ素（Si_3N_4）を積層し、厚さ300nmのゲート絶縁膜8を形成する。Si_3N_4以外にSiO_2，Ta_2O_5，Y_2O_3，TiO_3等を用いた場合も同様である。このように絶縁膜を多層構造にすることにより絶縁性を高めている。このゲート絶縁膜8の上に接して、プラズマCVD法によりアモルファスシリコンを30nmの厚みで積層し、半導体層9を形成する。この半導体層9の上に接して窒化ケイ素を200nmの厚みで積層し、フォトリソグラフィーによりエッチングストッパー層10をパターン形成する。エッチングストッパー層10のパターン化はフッ酸を用いてエッチングすることにより行なう。続いて、リンを添加したn⁺型アモルファスシリコンからなるコンタクト層11a、11bをプラズマCVD法により50nmの厚みで積層し、先に積層した半導体層9と共にフォトリソグラフィーによりこれらを同時にパターニングする。このときのパターン化はCF_4，O_2／Cl_2混合ガスを用いたドライエッチングにより行なう。さらにこの上にスパッタリング法でTi膜を形成し、フォトリソグラフィーにより信号線とソース電極12およびドレイン電極13とをパターン形成する。このときのパターン化はフッ硝酸を用いてエッチングすることにより行なう。以上により逆スタガー型と称されるTFTがエッチング保護膜5a上に作製される。

【0017】尚、上記構造で信号線とTFTのソース電極12およびTFTのドレイン電極13の材料としてはTiの他にAl、Cr、Mo等の金属を用いても良い。次に、このTi膜の上に酸化インジウムを主成分とした透明電極膜（ITO）を厚さ1000nmで成膜し、フォトリソグラフィーにより絵素電極14とこれを分岐させた付加容量（図示せず）とをパターン形成する。

【0018】このように製造されたTFTマトリクス基板は、エッチング保護膜5aとして酸化ケイ素あるいは酸化タンタルを用いた従来のTFTマトリクス基板に比べ、高い耐フッ酸性および耐ドライエッチング性が得られた。

【0019】

【発明の効果】以上、詳述したように、本発明によればエッチング保護膜を酸化アルミニウムにすることで、酸化ケイ素のエッチング保護膜でみられた低い耐フッ酸性および酸化タンタルのエッチング保護膜でみられた低い耐ドライエッチング性の両方を改善することができる。

【0020】従って、本発明のアクティブマトリクス配線基板では、エッチング工程による基板へのダメージが小さく、液晶表示装置として用いた場合のスイッチング素子の動作不良や断線等の発生も低減できる。

【図面の簡単な説明】

【図1】本発明の1実施例を示すTFTマトリクス基板

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のＴＦＴを含む部分での断面図。

【図２】従来の一般的なアクティブマトリクス基板の平面図。

【図３】従来のＴＦＴマトリクス基板のＴＦＴを含む部分での断面図。

【符号の説明】

1　ガラス基板
2　走査線
3　信号線
4　スイッチング素子
5ａ　エッチング保護膜（酸化アルミニウム）

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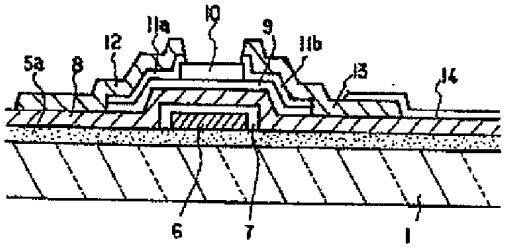
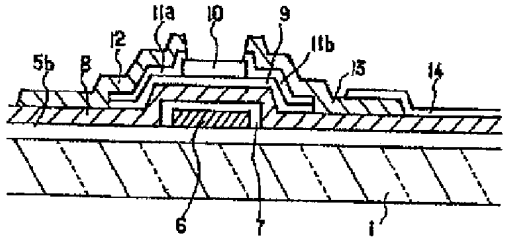
＊５ｂ　エッチング保護膜
6　ゲート電極
7　酸化絶縁膜
8　ゲート絶縁膜
9　半導体層
１０　エッチングストッパー層
１１ａ、１１ｂ　コンタクト層
１２　ソース電極
１３　ドレイン電極
１４　絵素電極

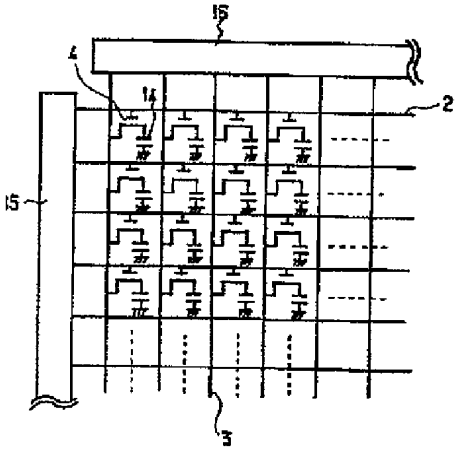
【図１】



【図３】



【図２】



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